WHAT IS CLAIMED IS:

Sub A1

1. A Hall device biasing circuit, comprising a plurality of terminals for applying a bias voltage to a plurality of Hall devices connected in series, respectively.

2. A Hall device biasing circuit according to claim 1, further comprising a constant voltage supply section for supplying a constant bias voltage to each of the plurality of terminals.

3. A Hall device biasing circuit according to claim 2, wherein the constant voltage supply section includes a constant voltage supply circuit in correspondence to the plurality of Hall devices.

4. A Hall device biasing circuit according to claim 2, wherein the constant voltage supply section includes:

a constant voltage supply circuit,

at least one current path through which a bias correction current flows from one of the plurality of terminals to another of the plurality of terminals, and

a correction current supply section for selecting one of the at least one current path based on a current

amount therein and adjusting the current amount in the selected current path to supply the bias correction current.

5. A Hall device biasing circuit according to claim 4, wherein the correction current supply section includes:

a constant voltage generation circuit, and

a comparison section connected to the at least one current path for selecting one of the at least one current path based on a current amount therein and adjusting the current amount in the selected current path based on a current amount flowing through the at least one current path and a current amount generated in the constant voltage generation circuit.

6. A Hall device biasing circuit according to claim 2, wherein the constant voltage supply section uses a supply voltage outside the Hall device biasing circuit.

7. A Hall device biasing circuit according to claim 2, wherein the constant voltage supply section includes:

at least one current path through which a bias correction current flows from one of the plurality of terminals to another of the plurality of terminals, and

a correction current supply section for selecting one of the at least one current path based on a current amount therein and adjusting the current amount in the selected current path to supply the bias correction current.

8. A Hall device biasing circuit according to claim 7, wherein the correction current supply section includes:

a reference voltage source, and

a comparison section connected to the at least one current path for selecting one of the at least one current path based on a current amount therein and adjusting the current amount in the selected current path based on a current amount flowing through one of the plurality of terminals and a current amount generated in the reference voltage source.

9. A Hall device biasing circuit according to claim 8, wherein the comparison section includes a comparator circuit.

10. A Hall device biasing circuit according to claim 9, wherein a positive terminal of the comparator circuit is connected to a terminal of one of the plurality of

terminals, and the negative terminal of the comparator circuit is supplied with a reference voltage generated in the reference voltage source.

11. A Hall device biasing circuit according to claim 9, wherein the comparator circuit includes a buffer amplifier.

12. A Hall device biasing circuit according to claim 7, wherein the at least one current path includes a switching device.

13. A Hall device biasing circuit according to claim 7, wherein the at least one current path includes an OR circuit and an inverter.

14. A Hall device biasing circuit according to claim 7, wherein the correction current supply section includes:

a plurality of reference voltage sources respectively provided in correspondence to the plurality of Hall devices, and

a plurality of comparison sections each connected to each of the at least one current path for selecting one of the at least one current path based on a current

amount therein and adjusting the current amount in the selected current path based on a current amount flowing through one of the plurality of terminals and a current amount generated in one of the plurality of reference voltage sources corresponding to the one of the plurality of terminals.

15. A Hall device biasing circuit according to claim 8, wherein the correction current supply section further includes a resistor between the reference voltage source and the comparison section for dividing a resistance of the reference voltage source.

16. A Hall device biasing circuit according to claim 11, wherein a former-stage terminal with respect to one of the plurality of terminals corresponding to the buffer amplifier is connected to a positive power supply of the buffer amplifier, and a latter-stage terminal with respect to the one of the plurality of terminals corresponding to the buffer amplifier is connected to a negative power supply of the buffer amplifier.

Sub A2 17. A magnetism detection circuit, comprising:

a plurality of Hall devices connected in series;

and

A2 Cont'd

a Hall device biasing circuit including at least a plurality of terminals corresponding to the plurality of Hall devices for supplying a constant bias voltage to each of the plurality of Hall devices respectively from the plurality of terminals.

18. A magnetism detection circuit according to claim 17, wherein the Hall device biasing circuit further includes a constant voltage supply section.

19. A magnetism detection circuit according to claim 17, wherein one end of the series of plurality of Hall devices is grounded.